

Performance Enhancement Techniques of a Banyan Network Based Interconnection Structure

Moustafa A. Youssef, Mohamed N. El -Derini, and Hussien H. Aly
Department of Computer Science and Automatic Control, Faculty of Engineering,
Alexandria University.

Abstract – In this paper two performance enhancement techniques namely the dilation and replication techniques which are commonly used with the standard banyan networks are applied to the Plane Interconnected Parallel Network (PIP). PIP is a switch introduced previously as a better banyan based interconnection structure. The performance of unbuffered and buffered modified PIP is analyzed analytically under uniform traffic model. We apply the simulation technique to verify the analytical results under the uniform traffic model and to study the performance of different heterogeneous traffic models. The performance is shown to increase significantly when the performance enhancement techniques are used which support the idea of using the switches based on these modifications as a new high performance ATM switches.

Index Terms – ATM switching, banyan networks, dilated networks, fast packet switching, replicated networks.

I-Introduction

Broadband ISDN (B-ISDN) allows the integration of different services over the same network. These services require different bandwidths and have different characteristics which lead to heterogeneous traffic over the network [1]. The design of large switches that can operate at high data transfer rates and meet the performance requirements of the different services applied to the network is a challenge.

Banyan networks are commonly used in multi-stage ATM switches because of their high degree of parallelism, self-routing, modularity, constant delay for all input-output port pairs, in-order delivery of cells, and suitability for VLSI implementation [2-8]. However, in banyan networks, there is only one path between each input and output port pair, and the edges of such a path are not dedicated. This means that other communicating pairs may share some links of a path connecting an input-output port pair.

The concern of this paper is to propose structures of new high performance ATM switches. We apply two performance enhancement techniques, namely the dilation and replication techniques, to the plane interconnected parallel network (PIP). The dilation and replication techniques were applied to the banyan network to enhance their performance [2,3]. PIP was introduced in [4] as a better banyan based interconnection structure. By applying the performance enhancement techniques to PIP, we take the advantage of dilation and replication which provide multiple paths from each input to each output, thus decreasing the effect of conflict between cells, and the advantage of PIP which gives better performance under heterogeneous traffic over the standard banyan network.

The outline of this paper is as follows: In section II, we describe the basic structure and operation of the Dilated and Replicated PIP switches. In section III, we study their performance under uniform and heterogeneous traffic models. We conclude the paper in section IV.

II-The Dilated and Replicated PIP Switch

II.1 Background

A cell switch is a box with N inputs and N outputs which routes the cells arriving at its input to their requested outputs. The general cell switch architecture is shown in Fig. 1. Several architectural designs have emerged to implement this switch. They may be classified into three categories: the shared-memory type, the shared-medium type, and the space-division type. Both shared-memory and shared-medium suffer from their strict capacity limitation, which is limited to the capacity of the internal communication medium. Any internal link is N times faster than the input link and it is usually implemented as a parallel bus. This makes such architectures more difficult to implement as N becomes large. Fig. 2 shows the shared-medium and shared-memory architectures.

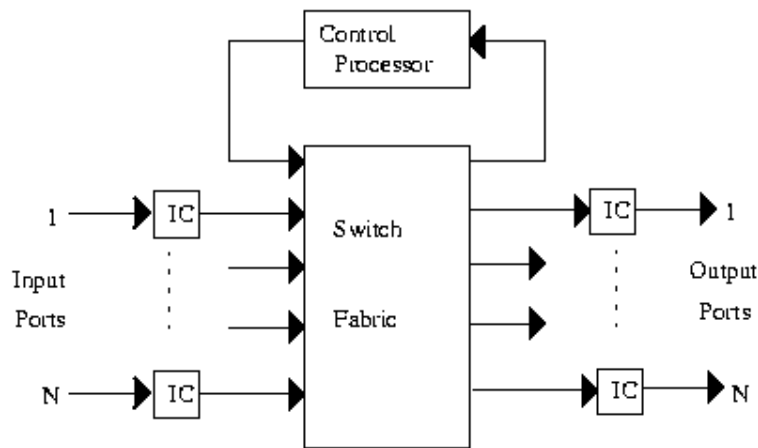


Figure 1. General Cell Switch Architecture

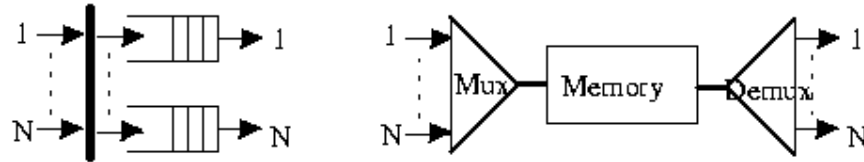


Figure 2. Shared Medium and Shared Memory Architectures

The simplest space-division switch is the crossbar switch, which consists of a square array of $N \times N$ crosspoint switches, one for each input-output pair as shown in Fig. 3. As long as there is no output conflict, all incoming cells can reach their destinations. If, on the other hand, there are more than one cell destined in the same timeslot to the same output, then only one of these cells can be routed and the other cells may be dropped or buffered. The major drawback of the crossbar switch stems from the fact that it comprises N^2 crosspoints, and therefore, the size of realizable such switches is limited. For this reason, alternative candidates for space-division switching fabrics have been introduced. These alternatives are based on a class of multistage interconnection networks called banyan networks [1].

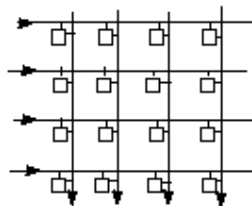


Figure 3. Crossbar Architecture

A banyan network consists of $n = \log_2 N$ stages (N is assumed to be a power of 2), each containing 2×2 switching elements (SE). Banyan networks have many desirable properties: high degree of parallelism, self-routing, modularity, constant delay for all input-output port pairs, in-order delivery of cells, and suitability for VLSI implementation. Their shortcoming remains blocking and throughput limitation. Blocking occurs every time two cells arrive at a switching element and request the same output link of the switching element. The existence of such conflicts (which may arise even if the two cells are destined to distinct output ports) leads to a maximum achievable throughput which is much lower than that obtained with the crossbar switch. An 8×8 banyan network is shown in Fig. 4.

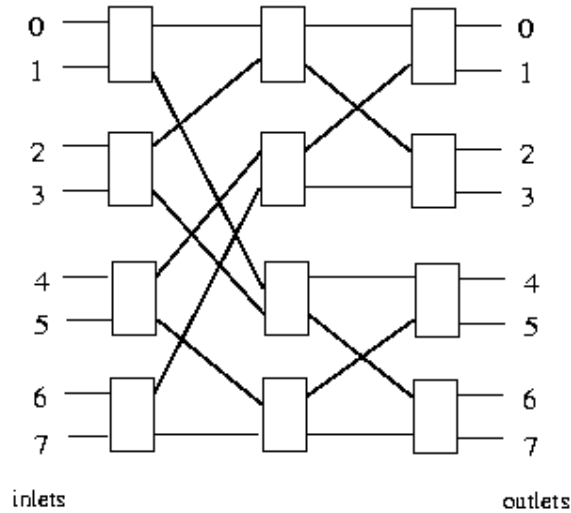


Figure 4. Banyan network

To overcome the performance limitations of banyan networks, various performance enhancing techniques have been introduced [2,3,6,7]. These techniques have been widely used in designing ATM switches [2-8].

The performance of banyan based switches depends on the applied traffic. As the applied traffic becomes heterogeneous, the performance of banyan based switches degrades drastically even if some performance enhancing techniques are employed.

In [4], the PIPN, a new banyan based interconnection structure is introduced. The PIPN exploits the desired properties of banyan networks while improving the performance by alleviating their drawbacks. In PIPN, the traffic arriving at the network is shaped and routed through two banyan network based interconnected planes. The interconnection between the planes distributes the incoming load more homogeneously over the network.

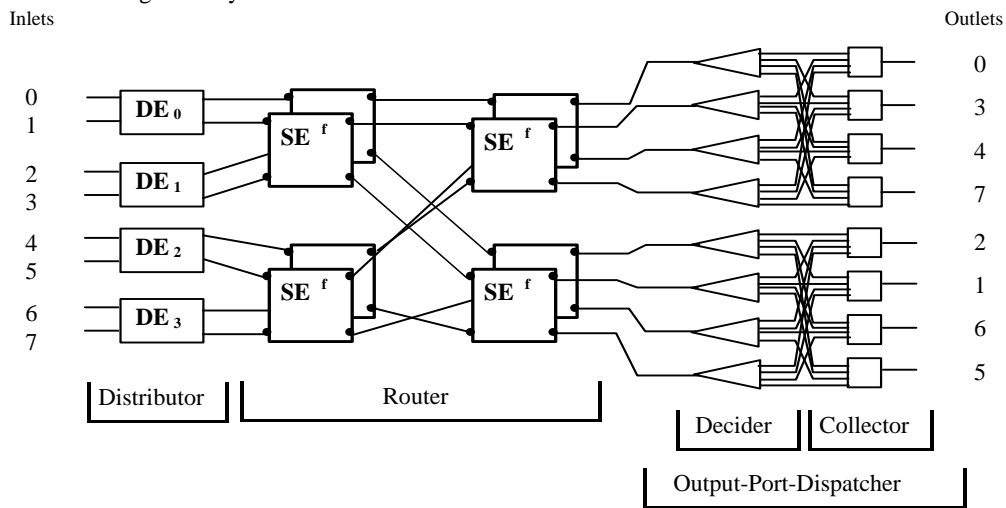


Figure 5. Complete structure of an 8x8 PIPN network

PIPN is composed of three main units, namely, the distributor, the router, and the output dispatcher as shown in Fig. 5 [4,5]. The cells arriving at the distributor divide the network into two groups in a random manner: the backplane and the front plane groups. The destination address fields of cells in one of the groups are complemented. The grouped cells are assigned to the router, which is a $N/2 \times N/2$ banyan network. The cells are routed with respect to the information kept in their destination address fields. Due to the internal structure of the router and the modifications in the destination address fields of some cells, an outlet of the router may have cells actually destined to four different output ports. The cells arriving from the outlets of the router are assigned to the requested output ports in the

output-port dispatcher [4,5]. The output-port dispatcher has two different sub-units: the decider and the collector. There is a decider unit for each router output and a collector unit for each output port. There are a total of N deciders and N collectors. The decider determines to which output port an arriving cell will be forwarded and restores its destination address field. Each collector has four inlets and an internal buffer to accommodate the cells arriving from four possible deciders.

II.2 The Dilated PIPN Switch Structure

One of the performance enhancement techniques of banyan networks is the dilation technique [2, 3]. In a dilated switching element, each link is replaced by K parallel links $K=2^i$ ($i=1,2,\dots$). Each SE can receive up to K packets at each of its input ports and it can forward at most K packets to any output. An 8×8 banyan network, implemented from 2×2 SE's for $K=2$ is shown in Fig. 6. To connect the input port of a SE to the output port of another, K independent links are used, so that up to K packets can be transferred simultaneously between two SE's in each clock cycle. The input of the first stage of the network receives a packet only on one of the K links, which is the input link of the network (the remaining $K-1$ links are unused). The packets on the K links at each output of all switches in the last stage of the network are multiplexed on a single link, which is the output link of the network. A network with dilation degree $=K$ is denoted by D_K .

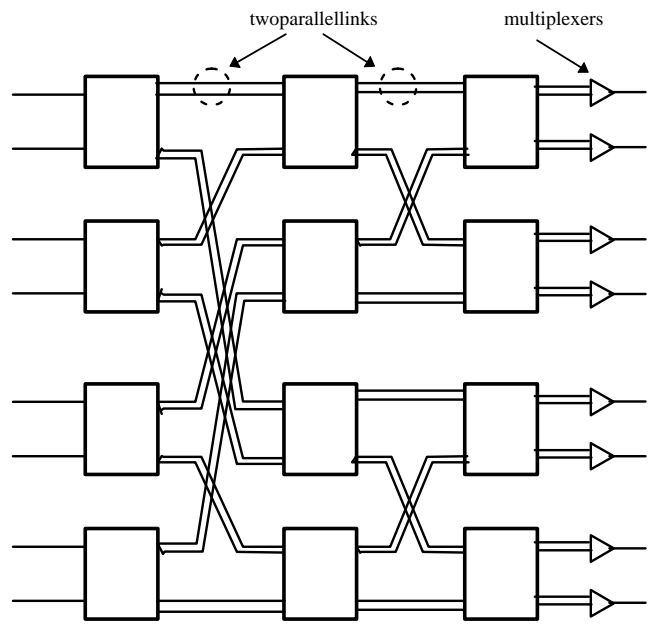


Figure 6. An 8×8 banyan network with double

The Dilated PIPN switch applies the dilation technique to the PIPN to benefit from the advantage of both techniques. Dilation provides multiple paths from each input to each output pair, thus decreasing the effect of conflict between packets. PIPN gives better performance under heterogeneous traffic over the standard banyan network.

The structure of the Dilated PIPN is shown in Fig. 7. It is shown from the figure that the structure of the Dilated PIPN is similar to the structure of the PIPN but with each SE replaced by a dilated and each link replaced by K parallel links.

SE

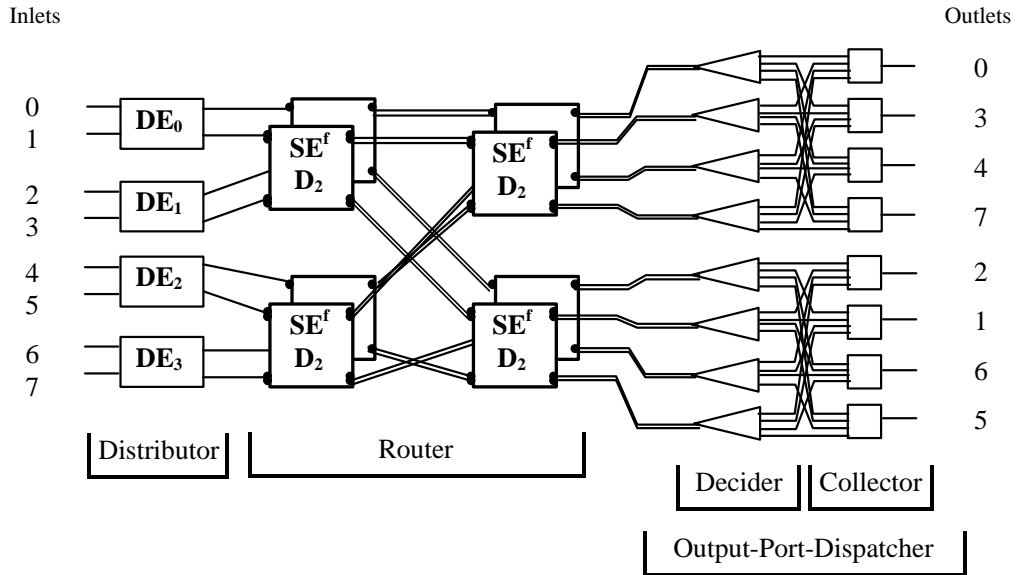


Figure 7. Complete Structure of an 8x8 Dilated PIPN Network for $K=2$ ($D=2$)

II.3 The Replicated PIPN Switch Structure

Another performance enhancement technique for banyan networks is the replication technique [2, 3]. Using the replication technique, we have $R=2^r$ ($r=1, 2, \dots$) parallel subnetworks. Each of these subnetworks is a banyan network. Two techniques are used to distribute the incoming cell over the R subnetworks. In the first technique, input of the switch is connected to input of each subnetwork by a 1-to- R demultiplexer. The demultiplexer forwards the incoming cells randomly across the subnetworks. Similarly, each output of a subnetwork is connected to the output of the switch through a R -to-1 multiplexer. If more than one cell arrive at the multiplexer, one of them is selected randomly to be forwarded to the output port and the others are discarded. This technique is called randomly loading parallel networks (R -to-1) [2, 3]. Fig. 8 shows a 4x4 randomly loaded banyan network constructed from two 4x4 banyan networks.

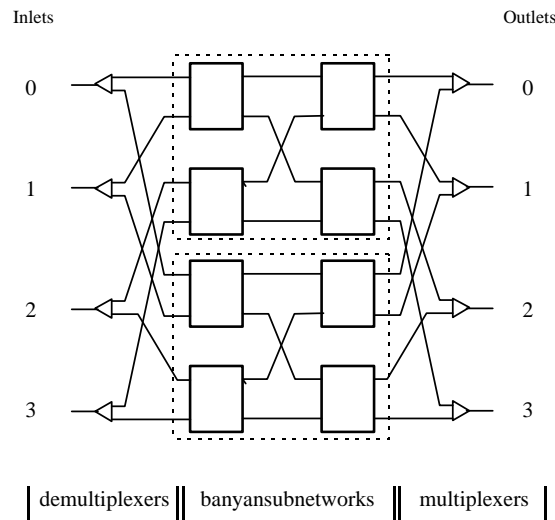


Figure 8. An 4x4 randomly loaded banyan network constructed from two 4x4 banyan networks

The second technique groups the outputs of the switch and assigns each group to one of the R truncated subnetworks. The i th input of the switch is connected to the i th input of each subnetwork through a

1-to-Rdemultiplexer. Thedemultiplexerforwardsincomingcellsaccordingtoitsrmostsignificantbits ofthedestinationaddressfield. Eachtruncatedsubnetworkhas r stages. Theoutputsofeachsubnetworkwhich aredestinedtothesameswitchoutputareconnectedvia an R -to-1multiplexertothisoutput. This techniqueiscalledselectivelyloadingparallel networks (SLPN) [2]. A 4x4selectivelyloadedparallel banyannetworkconstructedfromtwo4x4truncatedbanyannetworksisshowninFig.9.

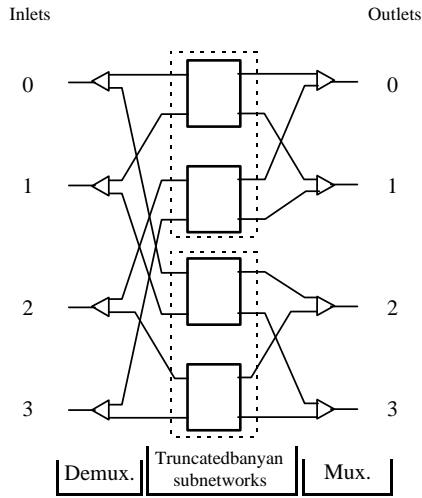


Figure 9.A 4x4selectivelyloadedbanyannetworkconstructed for two 4x4truncatedbanyannetworks

Similar to the Dilated PIPN, the Replicated PIPN switch allows multiple paths from each input to each output pair through the replication technique.

A 8x8 Randomly Loaded PIPN is shown in Fig. 10. It is shown from the figure that the Replicated PIPN is composed of RPIP N's connected in parallel. The structure of the Selectively Loaded PIPN is similar to the structure of the Randomly Loaded PIPN but the routers are truncated (have $r-1$ stages instead of r), and the demultiplexer forwards cells to subnetworks according to their most significant bits.

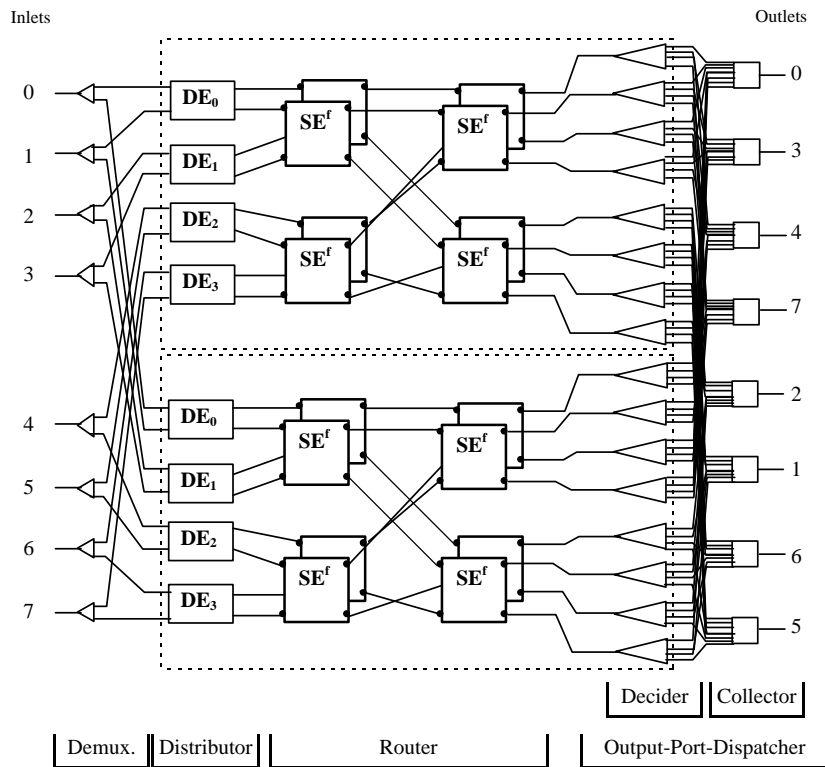


Figure 10. Complete Structure of an 8x8 Randomly Loaded PIPN Network

In all techniques, no multiplexers are needed at the output of the router as the deciders forward the incoming cells to the collectors' buffers.

III-Performance Evaluation of the Dilated and Replicated PIPN Switch

In this section, the normalized throughput of the Dilated and Replicated PIPN switch is evaluated. Analytical analysis is performed under uniform traffic model. For simulation, a Timed Colored Petri Net [9] is used to model the original and the Replicated PIPN. We begin by giving the Petri Net model of the SE.

III.1A Timed Colored Petri Net Model for the Dilated and Replicated PIPN SE

The structure of the Petri Net model is the same as that of the switches with each SE modeled as shown in Fig. 11.

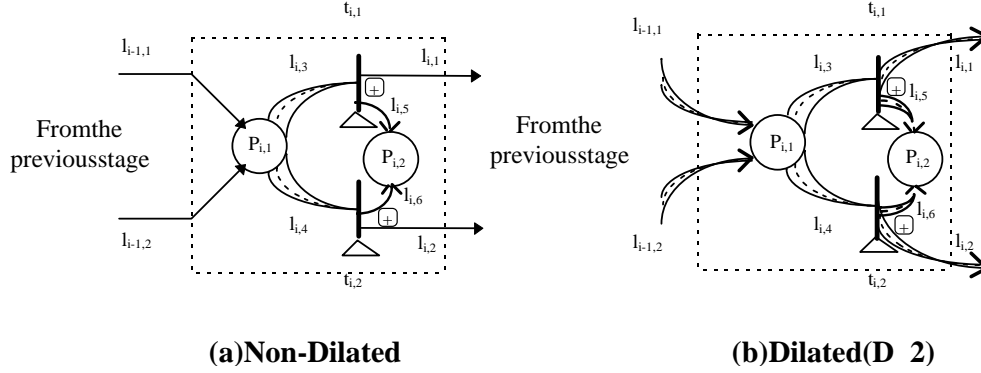


Figure 11. A Petri Net model for a SE

It is shown from the figure that links $l_{i-1,1}$ and $l_{i-1,2}$ represent the upper and lower inlets respectively while transitions $t_{i,1}$ and $t_{i,2}$ represent the upper and lower outlets. The place $p_{i,2}$ holds the cell that was dropped due to losing the contention.

The formal definition of the Petri Net model for the non-dilated SE is given as follows:

a-Structure

$$\begin{aligned}
 N &= (T, P, L, I, O, F) \\
 T &= \{t_{i,1}, t_{i,2}\} \\
 P &= \{p_{i,1}, p_{i,2}\} \\
 L &= \{l_{i-1,1}, l_{i-1,2}, l_{i,1}, l_{i,2}, l_{i,3}, l_{i,4}, l_{i,5}, l_{i,6}\} \\
 I: P \times T &\rightarrow L \\
 &I(p_{i,1}, t_{i,1}) = l_{i,3} \\
 &I(p_{i,1}, t_{i,2}) = l_{i,4} \\
 O: T \times P &\rightarrow L \\
 &O(t_{i-1,1}, p_{i,1}) = l_{i-1,1} \\
 &O(t_{i-1,2}, p_{i,1}) = l_{i-1,2} \\
 &O(t_{i,1}, p_{i,2}) = l_{i,5} \\
 &O(t_{i,2}, p_{i,2}) = l_{i,6}
 \end{aligned}$$

$F = \emptyset$
where the subscript i represents the stage number.

Two- Marking

We have only one type of tokens representing the cells:
 $K = (\text{destination address, other attributes})$

Three- Elements Definition

1-Transitions

Trans. No.	Type	I/P logic	O/P logic	Time fn.	Comments
$t_{i,1}$	Nonprimitive	Addressed ($K(0)=0$)	And	Const.	Switching time is const.
$t_{i,2}$	Nonprimitive	Addressed ($K(0)=1$)	And	Const.	Switching time is const.

2-Places

Place No.	Capacity	Queue Policy	Comments
$p_{i,1}$	2	n/a	Inlets
$p_{i,2}$	∞	n/a	AccumulatesDroppedCells

3-Links

Link	Type	Dimension	Priority	Comments
$l_{i-1,1}$	Transmitter	1	2	Upperinputfromthe previousstage
$l_{i-1,2}$	Transmitter	1	2	Lowerinputfromthe previousstage
$l_{i,1}$	Transmitter	1	2	Upperoutputtothenext stage
$l_{i,2}$	Transmitter	1	2	Loweroutputtothenext stage
$l_{i,3}$	Ordinary	Contents($p_{i,1}$) where $K(0)=0$	0	Carriescellsdestinedto upperoutlet
$l_{i,4}$	Ordinary	Contents($p_{i,1}$) where $K(0)=1$	0	Carriescellsdestinedto loweroutlet
$l_{i,5}$	Transmitter	1	1	Contentionresolutionlink
$l_{i,6}$	Transmitter	1	1	Contentionresolutionlink

TheelementdefinitionofthePetriNetmodelforthedilatedSEisgivenasfollows:

ElementsDefinition

1-Transitions

Trans. No.	Type	I/Plogic	O/P logic	Time fn.	Comments
$t_{i,1}$	Nonprimitive	Addressed($K(0)=0$)	And	Const.	Switchingtimeisconst.
$t_{i,2}$	Nonprimitive	Addressed($K(0)=1$)	And	Const.	Switchingtimeisconst.

2-Places

Place No.	Capacity	Queue Policy	Comments
$p_{i,1}$	2d	n/a	disthedilationdegree
$p_{i,2}$	∞	n/a	AccumulatesDroppedCells

3-Links

Link	Type	Dimension	Priority	Comments
$l_{i-1,1}$	Transmitter	$\text{Min}(\text{Contents}(l_{i-1,3}), d)$	2	Upperinputfromthe previousstage.Holdsupto dcells
$l_{i-1,2}$	Transmitter	$\text{Min}(\text{Contents}(l_{i-1,4}), d)$	2	Lowerinputfromthe previousstage.Holdsupto dcells
$l_{i,1}$	Transmitter	$\text{Min}(\text{Contents}(l_{i,3}), d)$	2	Upperoutputtothenext stage.
$l_{i,2}$	Transmitter	$\text{Min}(\text{Contents}(l_{i,4}), d)$	2	Loweroutputtothenext stage.
$l_{i,3}$	Ordinary	Contents($p_{i,1}$)where $K(0)=0$	0	Carriescellsdestinedto upperoutlet
$l_{i,4}$	Ordinary	Contents($p_{i,1}$)where $K(0)=1$	0	Carriescellsdestinedto loweroutlet
$l_{i,5}$	Transmitter	$\text{Cont}(l_{i,3}) - \text{Cont}(l_{i,1})$	1	Contentionresolutionlink
$l_{i,6}$	Transmitter	$\text{Cont}(l_{i,4}) - \text{Cont}(l_{i,2})$	1	Contentionresolutionlink

III.2 Performance Under the Uniform Traffic Model

In this section, we study the performance of the modified PIPN switches under uniform traffic model. In this model, packets are equiprobably destined to any output port. Thus, the load at the outlets of all SE's in the same stage will be the same.

The throughput of banyan networks, under uniform traffic model, was given in [2,3,5]. The performance of the original PIPN with sufficiently large buffer was studied in [4,5]. The performance of Dilated and Replicated banyan networks was studied in [2,3].

The buffers in PIPN are located in the collectors. In the following subsections, we perform buffer dimensioning analysis for the original PIPN and study the performance of the unbuffered and buffered Dilated and Replicated PIPN.

III.2.1 Unbuffered PIPN

The throughput of an $N \times N$ PIPN is achieved by an $N/2 \times N/2$ banyan network. This result is directly related to the number of stages since the traffic is uniform. In an $N \times N$ banyan network, there are n stages, however, in an $N \times N$ PIPN there are $n-1$ stages in the router [4,5]. The throughput of the original PIPN with sufficiently large buffer was studied in [4,5] and was given by:

$$X_{\text{banyan}} = 1 - \left(1 - \frac{X_{\text{PIPn}}}{2}\right)^2 \quad (\text{network of size } n) \quad (1)$$

where the throughput of a banyan network at stage i is given in [2,3,5] by:

$$X_i = 1 - \left(1 - \frac{X_{i-1}}{2}\right)^2 \quad \text{for } 1 \leq i \leq n \quad (2)$$

The throughput of an $N \times N$ unbuffered PIPN under uniform traffic can be found as follows:

Let X_{Router} denote the probability of finding a packet at the output of a router outlet ($X_{\text{Router}} = X_{\text{banyan of size } N/2 \times N/2}$). Since each output of the router can have packets destined to four different collectors, the probability of finding a packet at one input of a collector is $X_c = X_{\text{Router}}/4$. A collector can receive up to four packets at each clock cycle, then assuming buffer size = 0 for unbuffered PIPN, the throughput of an $N \times N$ unbuffered PIPN is given by:

$$X_{\text{unbuffered PIPN}} = 1 - \left(1 - X_c\right)^4 = \left(1 - \frac{X_{\text{banyan of size } N/2 \times N/2}}{4}\right)^4 \quad (3)$$

Where $X_{\text{banyan of size } N/2 \times N/2}$ is the throughput of a banyan network with $n-1$ stages.

Fig. 12 shows the simulation result for the original PIPN under uniform traffic model for various buffer sizes. The simulation and analytical results are consistent for buffer size equal zero. It is shown from figure that a buffer size of two per each collector is sufficient to achieve performance near infinite buffer. Thus this buffer size is chosen for testing the performance of modified PIPN switch under heterogeneous traffic types.

III.2.2 Unbuffered Dilated and Replicated PIPN Switches

The performance of an $N \times N$ unbuffered Dilated PIPN switch with dilation degree = K can be obtained as follows: Let $x_s(m)$ denote the probability of finding m packets on the output of a SE in stages (for $1 \leq s \leq n-1$) and let $x_0(m)$ denote the probability of finding m packets at the input of a SE in

stage 1 ($\sum_{m=0}^K x_s(m) = 1$, for $0 \leq s \leq n-1$). If X is the probability of finding a packet at every

input of the switch at each slot time, then X_{in} , the probability of finding a packet at each input of the router at each slot time, equals $X/2$. $x_s(m)$ and $x_s(K)$ can be calculated using the following equations [2,3]:

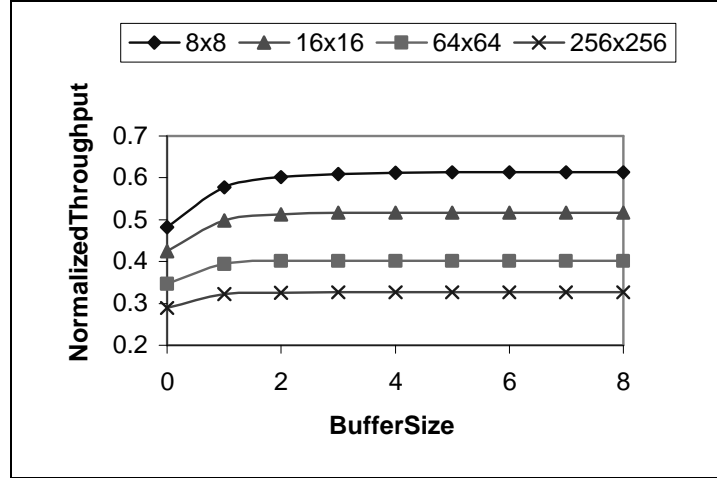


Figure 12. Effect of buffer size on PIPN performance at full load

$$x_0(0)=1 - X_{in}, x_0(1)=X_{in}, x_0(2)=x_0(3)=\dots=x_0(K)=0$$

$$x_s(m) = \sum_{i=0}^K \sum_{\substack{j=m-i \\ j \geq 0}}^K x_{s-1}(i)x_{s-1}(j) \binom{i+j}{m} 2^{-(i+j)} f \quad \text{orm} < K \quad (4)$$

$$x_s(K) = \sum_{i=0}^K \sum_{j=K-i}^K x_{s-1}(i)x_{s-1}(j) 2^{-(i+j)} \sum_{m=K}^{i+j} \binom{i+j}{m} \quad (5)$$

The values of $x_{n-1}(0), x_{n-1}(1), \dots, x_{n-1}(K)$ can be obtained by solving these recurrent relations. It is easy to prove that the output rate at each of the router outputs is $X_{Router} = \sum_{i=0}^K i \cdot x_{n-1}(i)$. Using the same reasoning as above, the throughput of an $N \times N$ unbuffered Dilated PIPN under uniform traffic can be given as:

$$P_{unbufferedDilatedPIP N} = 1 - \left(1 - \frac{X_{Router}}{4}\right)^4 \quad (6)$$

Fig. 13 shows the simulation and analytical results for the unbuffered Dilated PIPN under uniform traffic model.

The performance of an $N \times N$ randomly loaded banyan network was studied in [2] and [3] and was given by: $X_{out} = 1 - (1 - x_n)^R$ where x_n is the throughput of a banyan network having n stages with arrival rate equals X_{in} .

The performance of selectively loaded banyan network was studied in [2] and was given by:

$$X_{out} = 1 - (1 - x_{n-r})^R \quad \text{where } x_{n-r} \text{ is the throughput of a banyan network having } n-r \text{ stages with arrival rate equals } X_{in}.$$

Since the router of each subnet of the randomly loaded PIPN switch consists of $n-1$ stages, the output rate at each router's output link x_{n-1} can be obtained by the recurrence relation (2) with n equals X_{in} . Since each output of the router can have cells destined to four different collectors, the probability of finding a cell at one input of a collector is $X_c = x_{n-1}/4$. A collector can receive up to four cells at each clock cycle from each subnet, then the throughput of an $N \times N$ unbuffered randomly loaded PIPN is given by:

$$X_{unbufferedrandomly loadedPIP N} = 1 - (1 - X_c)^{4R} \quad (7)$$

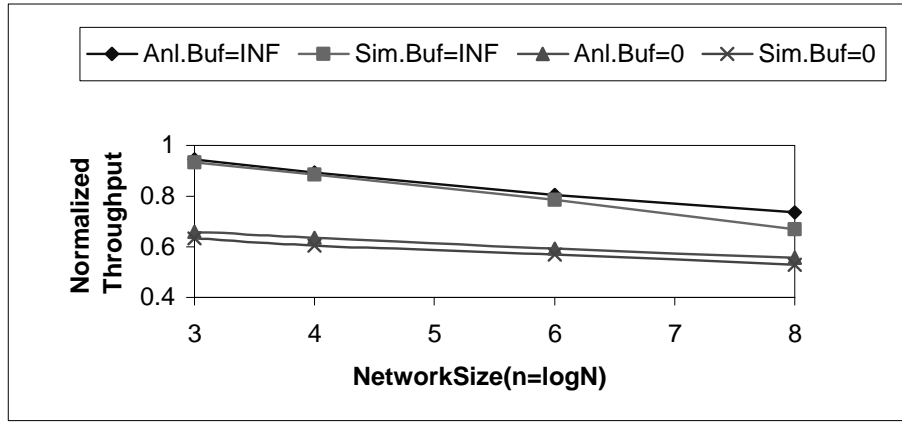
$$\begin{aligned} \therefore X_{\text{unbuffered randomly loaded PIPN}} &= 1 - \left(1 - \frac{X_{\text{banyanwit hn -1 stages a ndload =X}_{\text{in}}}}{4} \right)^{4.R} \\ &= 1 - \left(1 - X_{\text{unbuffered PIPN}} \right)^R \end{aligned} \quad (8)$$

where $X_{\text{unbuffered PIPN}}$ is the throughput of an $N \times N$ unbuffered PIPN with load equal X_{in} .
 Fig. 14.a shows the throughput of the unbuffered Randomly Loaded PIPN switch both analytically and by simulation.

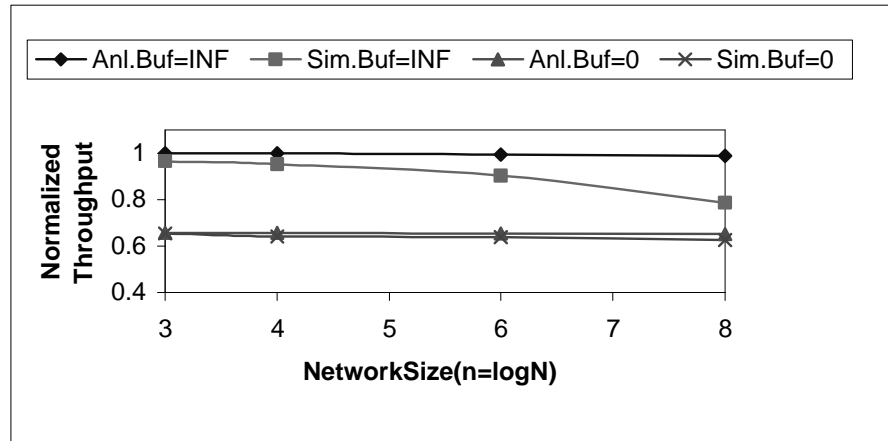
The throughput of an $N \times N$ unbuffered selectively loaded PIPN is similar to equation (8) but with $n-r-1$ stages instead of $n-1$.

$$\begin{aligned} X_{\text{unbuffered selective ly loaded PIPN}} &= 1 - \left(1 - \frac{X_{\text{banyanwit hn -r-1 stages}}}{4} \right)^{4.R} \\ &= 1 - \left(1 - X_{\text{unbuffered PIPN}} \right)^R \end{aligned} \quad (9)$$

where $X_{\text{unbuffered PIPN}}$ is the throughput of an $N/R \times N/R$ unbuffered PIPN with load equal X_{in} .
 Fig. 14.b shows the throughput of the unbuffered Selectively Loaded PIPN switch both analytically and by simulation.

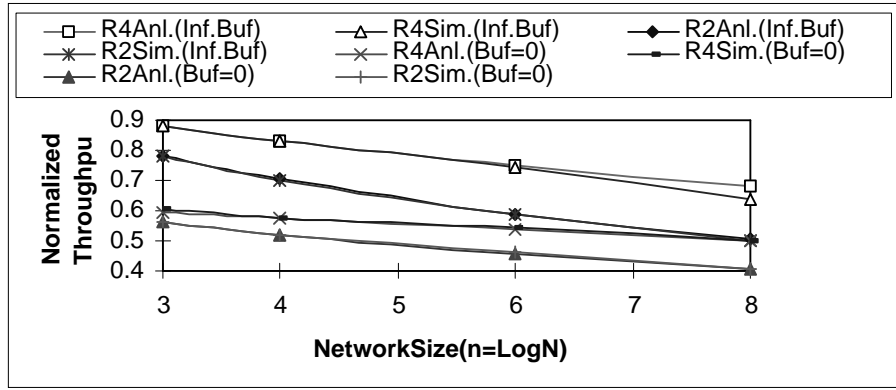


(a)D2

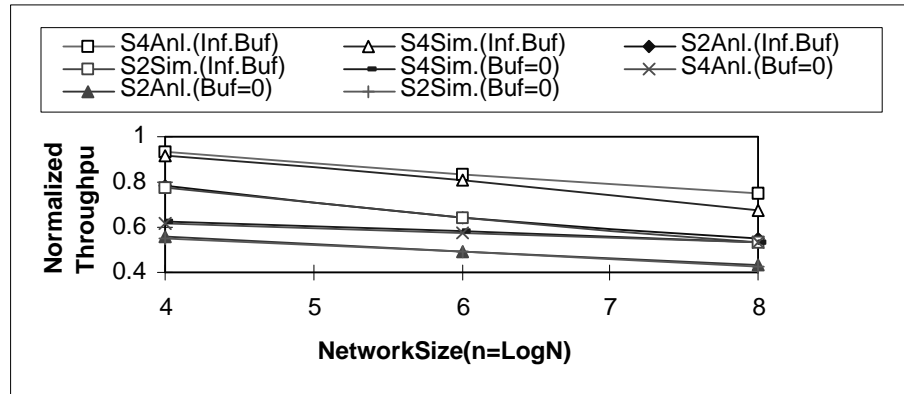


(b)D4

Figure 13. Analytical and simulation results for the Dilated PIPN under uniform traffic model (full load)



(a) Randomly Loaded (R_n)



(b) Selectively Loaded (S_n)

Figure 14. Analytical and simulation results for the Replicated PIPN under uniform traffic model (full load)

III.1.3 Buffered Dilated and Replicated PIPN Switches

Since there are no loss of cells under infinite buffer, the throughput of the Dilated PIPN switch is exactly as X_{router} in the unbuffered case above as there are no loss of cells.

The throughput of the randomly loaded Replicated PIPN switch under infinite buffer is exactly R times the throughput of a $N \times N$ PIPN with infinite buffer, given in equation (1).

$$X_{Randomly\ loaded\ PIPN\ with\ infinite\ buffer} = R \cdot X_{N \times N\ PIPN\ with\ infinite\ buffer} \quad (10)$$

Similarly, the throughput of the selectively loaded Replicated PIPN switch under infinite buffer is exactly R times the throughput of a $N/R \times N/R$ PIPN with infinite buffer, given in equation (1).

$$X_{Selectively\ loaded\ PIPN\ with\ infinite\ buffer} = R \cdot X_{N/R \times N/R\ PIPN\ with\ infinite\ buffer} \quad (11)$$

It is shown from figure 13 and 14 that the simulation curve departs from the analytical curve for the infinite buffer case especially for large network sizes. The infinite number of cells in the buffers justifies this difference as a large number of cells remain in the buffer waiting to be transmitted. This effect increases as the network size, dilation, and replication degrees increase.

Fig. 15 shows the throughput of D_2 and D_4 PIPN with buffer size equal to two cells per collector compared to the original PIPN with infinite buffer. Also the throughput of $R_2, R_4, S_2,$ and S_4 Replicated PIPN switches with buffer size of two cells per collector compared to the original PIPN with infinite buffer is shown in Fig. 16. It is shown from the figure that the throughput of these selectively loaded PIPN is better than that of the randomly loaded PIPN. This is expected as the former has fewer stages than the latter.

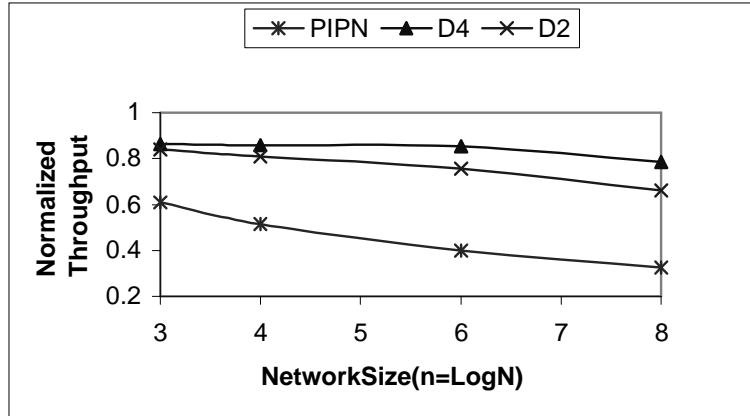


Figure 15. Performance of the Dilated and Original PIPN under uniform traffic model (full load)

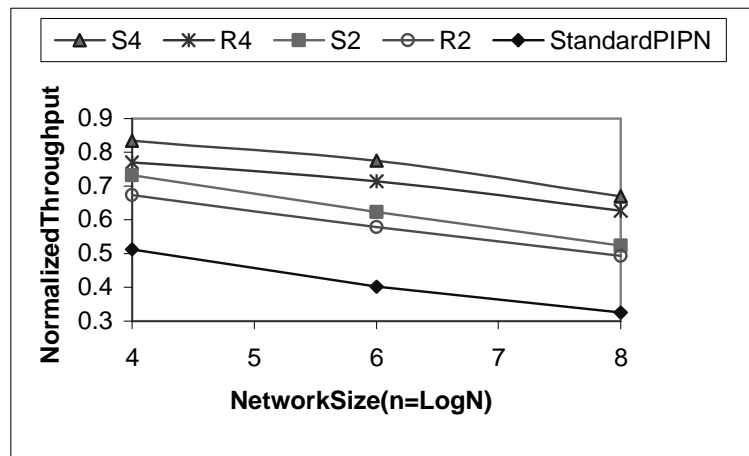


Figure 16. Performance of the Replicated and Original PIPN under uniform traffic model (full load)

III.2 Dilated and Replicated PIPN Performance Under Type -I Traffic Model

In Type -I traffic, output ports are grouped. The number of groups is an integer power of two. The ports in the same group have a equal chance of being selected by any incoming packet. However, each group may have a different selection probability. The parameters for the traffic type are selected to create heterogeneous outlet requests. The number of parameters is selected as eight since eight is a reasonable value for the number of outlet groups in the range 16 - 256 outlets [4,5]. In Fig. 17, the normalized throughput for $m=(0.3, 0.02, 0.15, 0.00, 0.20, 0.06, 0.22, 0.05)$ Type -I traffic with respect to varying incoming load and different network sizes is shown for the Dilated PIPN with $K=2$, Dilated PIPN with $K=4$, and the original PIPN. The percentage throughput improvement obtained by the Dilated PIPN is shown in Table 1.

Also the normalized throughput for the same Type -I traffic pattern with respect to varying incoming load and different network sizes for the $R_2, R_4, S_2,$ and S_4 Replicated PIPN switches, and the original PIPN is shown in Fig. 18. The percentage throughput improvement obtained by the Replicated PIPN is shown in Table 1.

It is shown from the figure that the difference between the D2 and D4, R2 and R4, S2 and S4 curves increases as the switch size increases. This is expected as when the switch size increases, the number of stages increases resulting in more contention. As, the dilation and replication degree increases, more paths are provided for the cells.

III.3 Dilated and Replicated PIPN Performance Under Type -II Traffic Model

In Type -II traffic, the inlets and the outlets are both divided into groups. Although the size of input groups is fixed, the output groups have different sizes. Moreover, the selection probability of an output port group varies depending on the input port number that sends the packet [4,5,10].

As proved in [10], Type -II traffic represented by more than $\lceil \log_4 N \rceil + 1$ parameters on a banyan network can be represented by using $\lceil \log_4 N \rceil + 1$ parameters only. Therefore, there is no need to test the performance of the modified PIPN under Type -II traffic represented by more than $\lceil \log_4 N \rceil + 1$ parameters.

The normalized throughput of the Dilated, Replicated and original PIPN switches of size 256×256 is evaluated under 19 patterns of Type -II traffic represented by four parameters within incoming load 1.0. The traffic patterns are varied between uniform traffic and the extreme heterogeneous case which is possible under the given traffic type and parameters. The aim is to present the behavior of both the modified switches and the original PIPN under various traffic patterns. The throughput for all Type -II traffic patterns are shown in Table 3 in appendix A.

The obtained results are summarized in Table 2. The tables show the maximum, minimum, average throughput values, and the standard deviation of each network type under the given traffic set. It is shown from this table that the dilation technique, when applied to PIPN, gives small throughput range (Max. - Min.) and a high average throughput. This small throughput range is a good indication for the consistency of the switching system as the Dilated PIPN performance does not fluctuate when the applied traffic varies.

The throughput of the selectively loaded PIPN is expected to be better than that of the randomly loaded PIPN as it has fewer stages. However, it is shown from the given Type -II patterns that the selectively loaded PIPN is not always superior over the randomly loaded (patterns 6 -19). Under heterogeneous traffic models, the selectively loading technique may overload some subnetworks, increasing the number of collisions, while leaving other subnetworks lightly loaded.

IV- Conclusions

In this paper, a high performance banyan based fast packet switches are introduced. The dilation and replication techniques are applied to the PIPN. These switches use the dilation and replication techniques to provide multiple paths between inputs and outputs and use the PIPN to smooth the heterogeneous traffic models. The existence of more paths between each input -output ports pairs make the modified switches more reliable than the original PIPN.

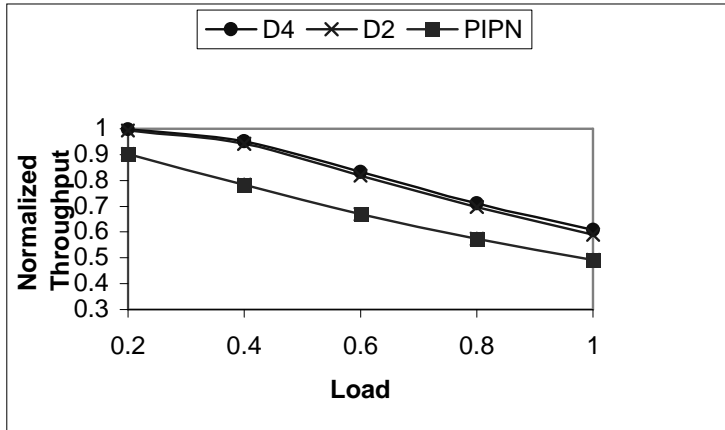
The performance of the modified PIPN is examined analytically and by simulation. It is shown that the modified PIPN gives better performance than the original PIPN under various traffic types. Buffer dimensioning analysis is performed to choose a suitable buffer size.

The performance of two techniques for distributing cells among the subnetworks of the Replicated PIPN is examined. The analysis shows that selectively loading technique is better than the randomly loading technique under uniform traffic model. This is due to the fewer number of stages in the former technique. However, under heterogeneous traffic models, the randomly loading technique becomes better than the selectively loading technique as the second technique may overload some subnetworks while others subnetworks are lightly loaded causing more contention in the overloaded subnetworks while the randomly loading technique distributes incoming cell sequi probably among the subnetworks.

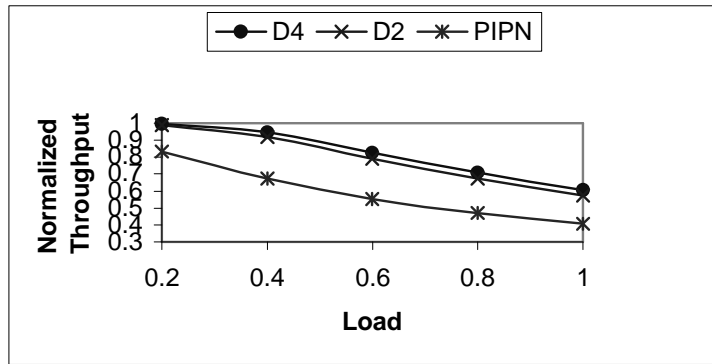
The dilation technique is found to be superior to the replication technique. This is expected as the dilation technique offers a link state at each outlet of the SE in all stages while the replication technique distributes the incoming cells over the networks at the first stage.

The resulting switches have a significant increase in performance under homogeneous and heterogeneous traffic models which supports the idea of fusing them as a new fast packet switch.

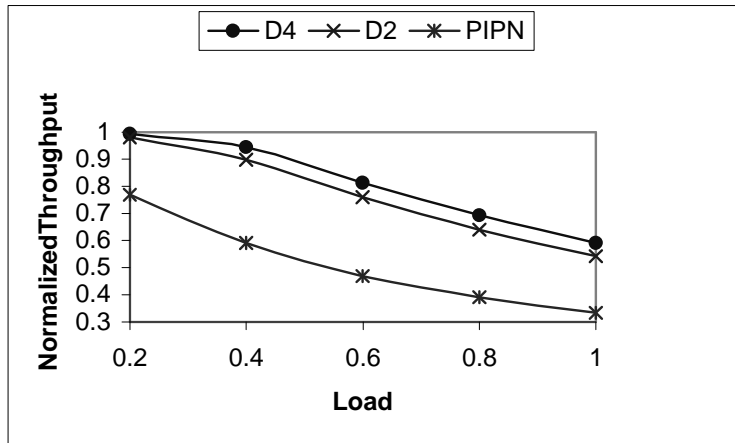
For future work, the performance of the switch can be tested under other arrival traffic models. The implementation aspects of the switches, such as cost and reliability, may be studied in more detail.



(a)N=16

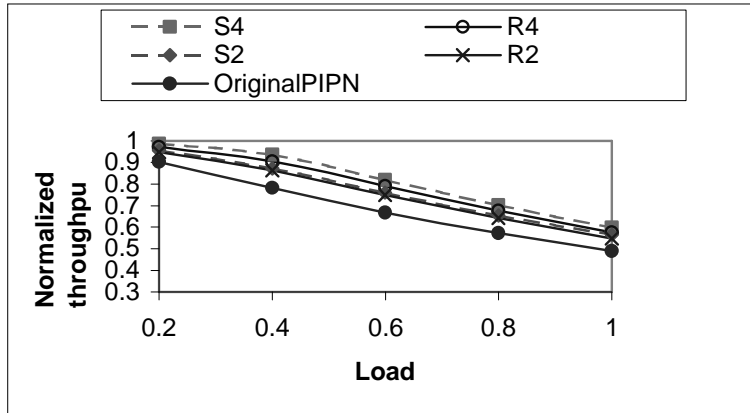


(b)N=64

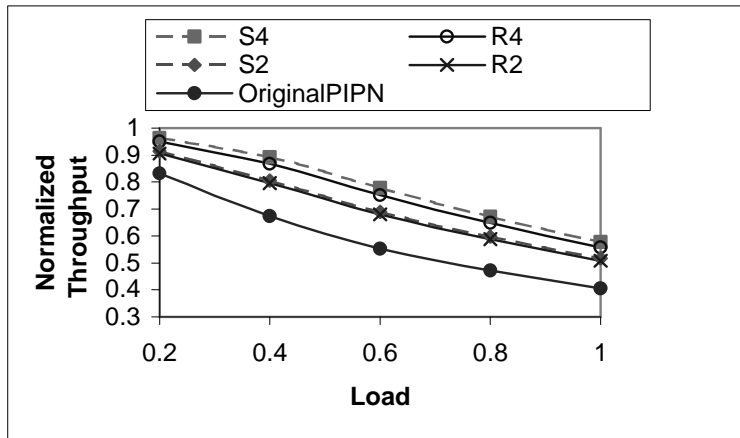


(c)N=256

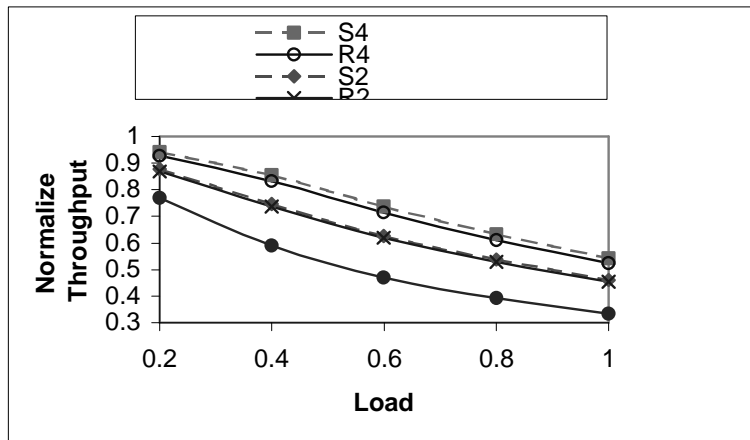
Figure 17. Performance under (0.30, 0.02, 0.15, 0.00, 0.20, 0.06, 0.22, 0.05) Type -I traffic for different network sizes



(a)N= 16



(b)N=64



(c)N=256

Figure18.Performanceunder (0.30,0.02,0.15,0.00,0.20,0.06,0.22,0.05)Type -I trafficfordifferentnetworksizes

Table 1 Average Percentage Throughput Improvement for the Dilated and Replicated PIPN over the Original PIPN for Type -I Traffic Pattern (0.3, 0.02, 0.15, 0.00, 0.20, 0.06, 0.22, 0.05)

Network Size	D2	D4	R ₂	S ₂	R ₄	S ₄
16x16	18.9	20.9	10.2	12.1	15.5	19.2
64x64	36.5	41.8	20.0	21.7	30.9	34.8
256x256	53.3	63.3	28.2	29.9	45.3	49.6

Table 2 Summary of Performance Results for 256x256 Dilated, Replicated, and original PIPN Under Different Type -I Traffic Patterns

Network Type	PIP _N	D2	D4	R2	S2	R4	S4
Min.	0.2571	0.6272	0.8074	0.4425	0.3154	0.6121	0.3914
Max.	0.3216	0.7107	0.8345	0.4943	0.5298	0.6452	0.6937
Average	0.3040	0.6772	0.8266	0.4823	0.4094	0.6365	0.5494
Max.-Min.	0.0645	0.0835	0.0270	0.0517	0.2143	0.0330	0.3023
Std.Deviation	0.0201	0.0214	0.0066	0.0156	0.0722	0.0097	0.0955

References

- [1] M. De Prycker, Asynchronous Transfer Mode Solution for Broadband ISDN. (U.K.: Ellis Horwood Ltd., 1991).
- [2] Manoj Kumar and J. R. Jump, "Performance of unbuffered shuffle exchange networks," IEEE Trans. Comput., vol. C-35, no. 6, June 1986.
- [3] Clyde P. Kruskal and Marc Snir, "The performance of multistage interconnection networks for multiprocessors," IEEE Trans. Comput., vol. C-32, no. 12, Dec. 1983.
- [4] Sema F. Oktug and Mehmet U. Caglayan, "Design and performance evaluation of a banyan network based interconnection structure for ATM switches," IEEE J. Select. Areas Commun., vol. 15, no. 5, June 1997.
- [5] Sema F. Oktug and Mehmet U. Caglayan, "Design and performance evaluation of a banyan network-based interconnection structure for ATM switches," Ph.D. dissertation, Bogazici Univ., Istanbul, Turkey, Spring 1996.
- [6] Fouad A. Tobagi, Timothy Kwok, and Fabio M. Chiussi, "Architecture, performance, and implementation of a banyan ATM switch," IEEE J. Select. Areas Commun., vol. 9, Oct. 1991.
- [7] Debashis Basak, Abhijit K. Choudhury, and Ellen L. Hahne, "Sharing memory in a banyan-based ATM switch," IEEE J. Select. Areas Commun., vol. 15, no. 5, June 1997.
- [8] James N. Giacomelli, Jason J. Hickey, William S. Marcus, W. David Sincoskie, and Morgan Littlewood, "Sunshine: a high performance self-routing broadband cell switch architecture," IEEE J. Select. Areas Commun., vol. 9, no. 8, Oct. 1991.
- [9] Hussien H. Aly, Khalil M. Ahmed, and M. Salah Selim, "Timed Colored Petri Nets (TCPN)," Advances in Modeling and Simulation, AMSE Press, Vol. 1, No. 4, 1984, pp. 11-20.
- [10] Sema F. Oktug and Mehmet U. Caglayan, "Parameter threshold type -I traffic for banyan networks," Elect. Lett., vol. 32, Feb. 1996.

Appendix A

Here we list the patterns of Type-II traffic model used to compare the performance of the modified and original PIPN [4,5].

Table 3 Throughput of 256x256 Dilated, Replicated and original PIPN Under Various Type-II traffic Patterns

No	Type-II Traffic	PIPN (thr)	D2 (thr)	D4 (thr)	R ₂ (thr)	S ₂ (thr)	R4 (thr)	S ₄ (thr)
1	(0.12,0.13,0.25,0.50)	0.3214	0.6847	0.8258	0.4943	0.5298	0.6418	0.6937
2	(0.05,0.05,0.45,0.45)	0.3188	0.6899	0.8303	0.4930	0.5280	0.6438	0.6656
3	(0.05,0.45,0.10,0.40)	0.3114	0.6762	0.8277	0.4861	0.5173	0.6385	0.6485
4	(0.45,0.05,0.05,0.45)	0.3108	0.6766	0.8300	0.4857	0.5211	0.6389	0.6404
5	(0.00,0.20,0.00,0.80)	0.3190	0.6771	0.8148	0.4907	0.4791	0.6369	0.6353
6	(0.45,0.05,0.40,0.10)	0.3170	0.6721	0.8323	0.4889	0.4185	0.6407	0.6159
7	(0.40,0.30,0.20,0.10)	0.3144	0.6887	0.8264	0.4903	0.4168	0.6420	0.5696
8	(0.30,0.00,0.60,0.10)	0.3175	0.6839	0.8326	0.4917	0.4154	0.6426	0.5970
9	(0.50,0.25,0.15,0.10)	0.3079	0.6869	0.8307	0.4853	0.4159	0.6402	0.5511
10	(0.05,0.45,0.45,0.05)	0.3189	0.6771	0.8319	0.4907	0.3873	0.6420	0.5948
11	(0.00,0.00,0.00,1.00)	0.3216	0.6754	0.8074	0.4914	0.3541	0.6336	0.5614
12	(0.25,0.25,0.50,0.00)	0.3204	0.6905	0.8344	0.4941	0.3536	0.6452	0.5647
13	(0.70,0.15,0.10,0.05)	0.2936	0.6715	0.8311	0.4731	0.3718	0.6342	0.4882
14	(0.45,0.45,0.05,0.05)	0.2988	0.7040	0.8313	0.4848	0.3810	0.6429	0.4614
15	(0.00,0.20,0.80,0.00)	0.3118	0.6918	0.8258	0.4901	0.3522	0.6420	0.5148
16	(0.80,0.10,0.06,0.04)	0.2843	0.6548	0.8228	0.4639	0.3522	0.6246	0.4610
17	(0.00,0.00,1.00,0.00)	0.2918	0.7107	0.8230	0.4836	0.3538	0.6400	0.3924
18	(1.00,0.00,0.00,0.00)	0.2574	0.6271	0.8234	0.4425	0.3154	0.6126	0.3914
19	(0.00,1.00,0.00,0.00)	0.2571	0.6273	0.8233	0.4436	0.3157	0.6121	0.3915